A CMOS Transmit/Receive IF Chip-Set for WCDMA Mobiles

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Abstract — **A transmit/receive IF chip-set integrating modulator/demodulator and AGCs for WCDMA mobiles in 0.35μm CMOS process is presented. Circuit innovations that achieve linear-in-dB gain control for wide-dynamic range AGCs with compensation against temperature and process variations to meet stringent specifications overcoming the limitations of CMOS technology are reported.**

I. Introduction

IF circuits for 3G wireless receivers like WCDMA with a high frequency AGC function and stringent specifications have traditionally been implemented using Bipolar/BiCMOS processes [1] owing to the problems of mismatch, gain-bandwidth and reproducibility associated with a conventional CMOS process. Some reported CMOS implementations, however, rely on an enhanced digital content to overcome such difficulties [2]. However, such an approach requires high-speed ADCs that are difficult to design. At low frequencies, precise analog requirements are met in CMOS technology using negative feedback, trading off voltage gain. However this technique cannot be readily applied to high frequency high gain amplifiers because of stability restrictions which usually require the gain-bandwidth to be reduced. Therefore, alternate means of stabilising gain must be found. Additionally, currently available CMOS devices exhibit adequate high frequency performance only if short channel, and in some cases, minimum channel length devices are used. The performance of high frequency precision differential CMOS analog circuits, therefore, suffers heavily due to transistor mismatches.

Overcoming such problems with innovative circuit techniques, we have achieved a high level of performance coupled with the highest integration level known to us for WCDMA IF transmit/receive chip-sets in CMOS technology using a 0.35μm, 2-poly, 3-metal process. The transmit-chip integrates an AGC amplifier, a quadrature modulator (up-converter) and a buffer for driving 50Ω off-chip load. The AGC circuit involves new techniques to realise a precise linear-in-dB gain control characteristic. This characteristic is further compensated against temperature and process variations using a new gain compensating bias generator. The novel inductor-less 50Ω buffer features unity gain which is difficult to achieve since CMOS source followers are known to exhibit huge signal losses because of inadequate transconductance. The receive-chip integrates another AGC amplifier and a quadrature demodulator (down-converter). Both chips are equipped with quadrature LO generators while operating from a single power supply of 3.0V ±10% for an ambient operating temperature of –30°C to +85°C. The demodulator and LO amplifiers also use a new approach – capacitively source coupled differential stages – to suppress DC offsets. The chips have a core die size of 1.5mm^2 each.

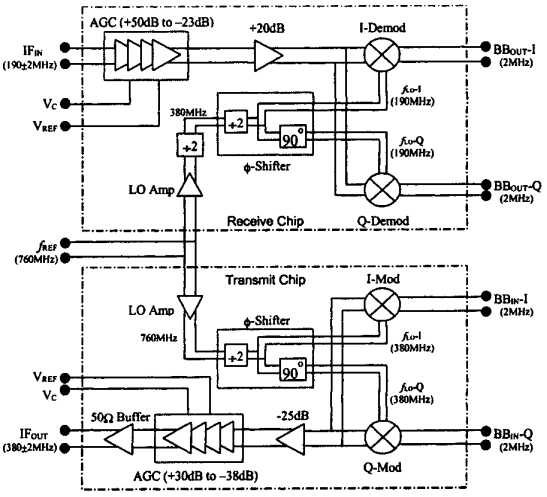

Fig. 1. Block Diagram of WCDMA Transmit/Receive chipset.

II. Circuit Description

A. Block Diagram

Fig. 1 shows the block diagram of the system. The transmit signal path contains the I/Q modulator, a 25dB attenuator and an AGC amplifier with a dynamic range of 68dB. The operating frequency range of this path is

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380MHz (transmit IF frequency) ± 2MHz (base-band frequency). A quadrature LO generator generates f_{LO}-I and f_{LO}-Q for the modulator from a 760MHz reference source f_{REF}. The receive signal path begins with a 73dB dynamic range AGC amplifier followed by a 20dB gain amplifier and an I/Q demodulator. The operating frequency of the receive path is 190MHz (receive IF frequency) ± 2MHz. A LO generator generates the required quadrature signals for the demodulator from f_{REF}.

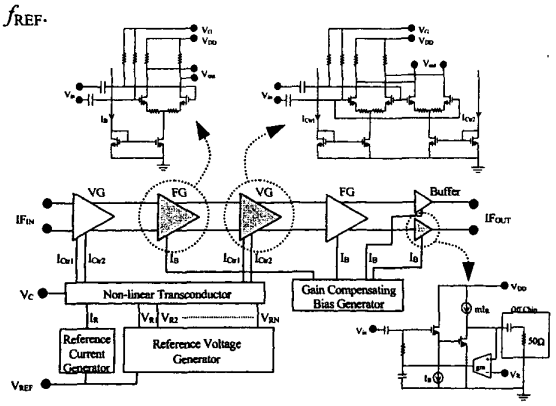

Fig. 2. Amplifiers and Buffer for AGC section.

B. AGC Amplifier and 50Ω Buffer

The overall architecture of the AGC amplifiers is shown in Fig. 2. It is organised as a cascade of alternating fixed (FG) and variable gain (VG) blocks for a good compromise between signal handling and noise. The VG block design is based on Gilbert cell topology - the gain variation being obtained by adjusting the differential of the bias currents I_{Ctr1} and I_{Ctr2}. DC blocking capacitors prevent propagation and amplification of DC offset voltages. The low input capacitance buffer has a unity voltage gain while driving external 50Ω load. This is achieved using a source-follower and common-source amplifier combination with relatively small size and power consumption. The DC voltage at the output is stabilised using an active feedback with a g_m-C filter to selectively allow DC feedback. The overall frequency response of the entire AGC amplifier chain is flat within ±0.25dB for the operating frequency range. This requires the individual amplifier blocks in the chain to have 3-dB bandwidths in the range of 600-900MHz.

The bias currents for the VG stages are obtained from a non-linear transconductor, shown in Fig. 3. It converts the control voltage input V_C into identical sets of differential currents (with a fixed common-mode) such that the overall gain of the chain A_V varies in linear-in-dB fashion with V_C. The reference voltage generator generates several reference voltages V_{R1}-V_{RN} for the non-linear transconductor, with magnitudes in-between the control voltage range of V_C, from a single

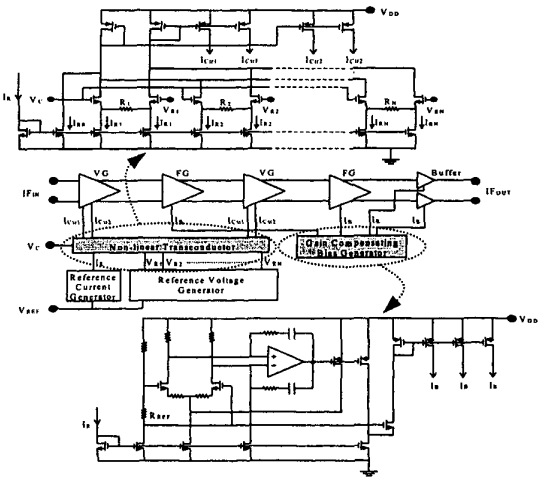

Fig. 3. Gain control and compensation circuitry for AGC section.

temperature independent reference input V_{REF}. The reference current generator feeds a nearly temperature independent reference current I_R generated from V_{REF} to the non-linear transconductor. By appropriate choice of V_{R1}-V_{RN} and I_{R0}-I_{RN} and R_1-R_N, the required non-linear characteristic is obtained. Since the characteristics of short-channel MOS devices used in the VG stages are difficult to predict with simple equations, this approach can result in a more linear (in dB) gain control characteristic compared to that described in [3].

The bias current for the FG stages as well as the buffer is obtained from the gain compensating (GC) bias generator, also shown in Fig. 3. It incorporates a feedback loop to force the transconductance of a differential pair, of the same type as in the FG stages, to be inversely proportional to an on-chip resistor R_{REF}. The circuit outputs the bias current I_B of the differential pair which, when used to bias the transistors of the FG stages and the buffer, helps to maintain a constant voltage gain for them. This results in a stable gain control characteristic, irrespective of process parameter and temperature variations.

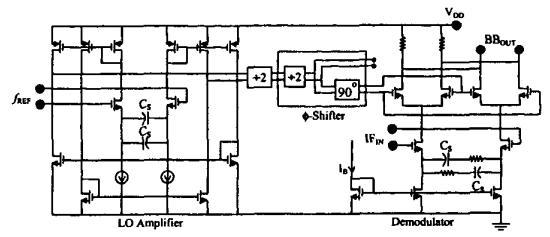

Fig. 4. LO amplifier and demodulator circuits

C. The Modulator and Demodulator

The modulator and demodulator designs are based on Gilbert cell topology. The channel lengths and the layouts of the differential devices and load resistors are carefully optimised to reduce mismatches causing imbalances in the circuits. The circuits are also biased using current from the GC bias generator to stabilise their gains against process and temperature variations. The LO phase shifter uses SCL flip-flops to generate quadrature LO signals by halving the input frequency. The low frequency base-band output of the demodulator needs to have very small DC offset for direct coupling to the following stage. The DC offset of the LO amplifier also needs to be small for proper operation of the flip-flops. Fig. 4 shows how such problems have been addressed using source coupling capacitors C_S of selected differential transistor pairs.

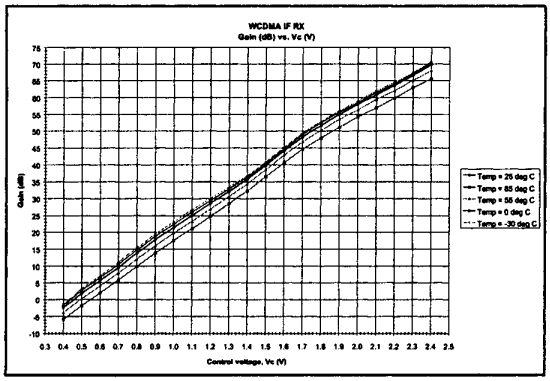

Fig. 5. Gain control characteristics of the receive-chip

III. Measurement Results

The transmit-chip gain was measured to be -5dB to -73dB for V_C ranging from 0.4V to 2.4V. The corresponding figures for the receive-chip were +70dB to -3dB. The deviation of each characteristic for the specified temperature range was within +1dB to -4dB as shown in Fig. 5. For the transmit-chip, the measured LO, sideband and 3rd harmonic suppression was -38dBc, -44dBc and –48dBc respectively at maximum gain as shown in Fig. 6. The output I/Q amplitude and phase mismatches for both transmit and receive sections were measured to be less than 1.0dB and ±2° respectively. The measured supply current for the transmit and receive chips were 31mA and 17mA respectively with a standby current not exceeding 10μA for each. The chip-set microphotograph is shown in Fig. 11.

Fig. 7 shows the deviation of the overall gain control characteristics of the transmit-chip from the ideal linear-in-dB characteristic. It can be seen from this plot that the deviation measured is within +/-2.0dB. The input P1dB (at maximum gain) measurement for this chip is 1.5dBm as shown in Fig. 8.

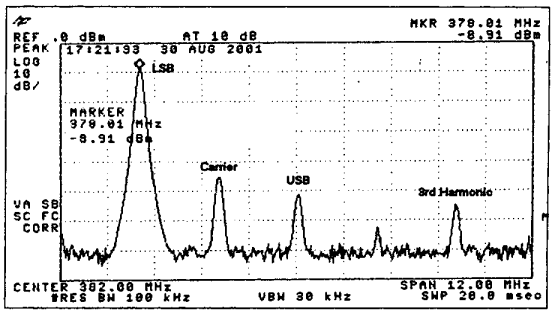

Fig. 6. Output spectrum of the transmit-chip with single component base-band signal

Fig. 9 plots the deviation of the overall gain control characteristics of the receive-chip from the ideal linear-in-dB characteristic superimposed. It can be seen from this figure that the deviation measured is within +/-2.0dB. The input P1dB (at maximum gain) measurement for this chip is –67.35dBm as depicted in Fig. 10. A summary of measured results is shown in Table 1.

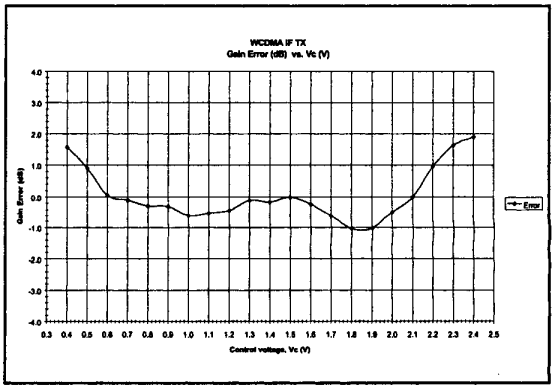

Fig. 7. Linearity error of gain control characteristic for transmit-chip

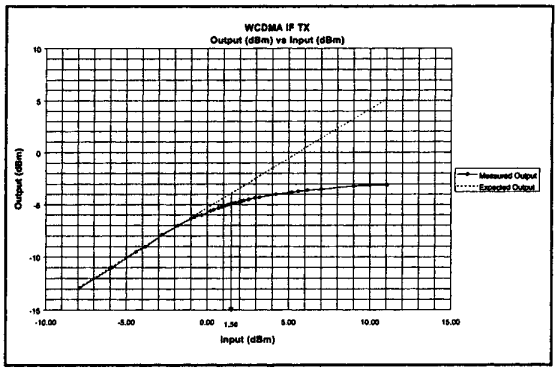

Fig. 8. Input P1dB at maximum gain for transmit-chip

TABLE 1
SUMMARY OF MEASURED RESULTS/PARAMETERS FOR WCDMA IF CHIP-SET

Parameter	Transmit-chip	Receive-chip	Units
LO frequency	380.0	190.0	MHz
IF frequency	380.0±2.0	190.0±2.0	MHz
Base-band frequency	0-2.0	0-2.0	MHz
Reference frequency	760.0	760.0	MHz
Maximum gain @ V_C=2.4V	-5.0	70.0	dB
Minimum gain @ V_C=0.4V	-73.0	-3.0	dB
Dynamic range/Linearity error	68.0/±2.0	73.0/±2.0	dB/dB
Input P1dB (at max. gain)	1.5	-67.35	dBm
LO suppression	-35.0		dBc
Sideband suppression	-46.0		dBc
3rd harmonic suppression	-47.0		dBc
I/Q amplitude mismatch		< 1.0	dB
I/Q phase error		±2.0	degrees
Supply voltage V_{DD}	3.0±10%	3.0±10%	V
Supply current – active/standby	31.0/< 10.0	17.0/< 10.0	mA/μA
Core die area	1.5	1.5	mm^2

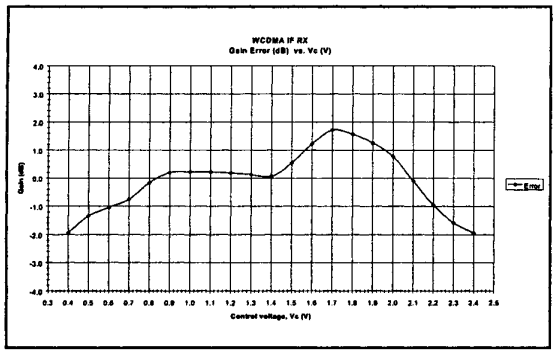

Fig. 9. Linearity error of gain control characteristic for receive-chip

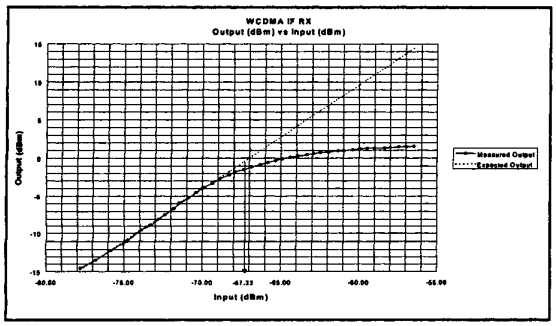

Fig. 10. Input P1dB at maximum gain for receive-chip

IV. CONCLUSION

A 0.35μm CMOS implementation of the IF sections for WCDMA transceivers has been presented. Stringent specifications have been met by using minimum channel length NMOS devices in frequency critical parts of the circuits. Special circuit techniques have been applied to overcome the associated problems of mismatch, linearity, temperature and process variations for such short-channel devices. The measurement results show that such techniques have been successfully applied.

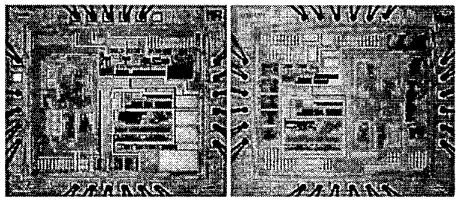

Fig. 11. The chip-set microphotograph

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